

High Speed Board Design & Signal Integrity Course

Course Number 735 – 48 Hours

Overview

Contemporary components employ advanced technologies to achieve high speeds. Hence, most new applications are advanced High Speed systems. Those high speed signals sometimes act like RF signals, whereas most Hardware Engineers are equipped with more than 20 years old "rules of thumb".

- Are the "rules of thumb" valid in your application?
- Do you know on which assumptions are they based?
- Do you know their origins?
- Do you understand them?
- Do they comply with your system requirements?

The High Speed Board Design Course explores the High Speed Media and Technologies, based on academic facts, design examples, simulation examples, DEMOs, and hands-on Workshops.

This course is essential for Hardware Design Engineers who seek to tell apart the superstitious beliefs from physical facts.

On Completion, Delegates will be able to

The participant will acquire:

- Academic & Technical knowledge on the studied material
- Guidelines and rules for hands on applications
- Tools to cope with "daily" problems by choosing the most suitable solution

The participant will get acquainted with:

- "Daily" problems & Solutions
- Technical Definitions for terms related with High Speed
- Contemporary tools / calculators used for hardware design

Asking questions to better understand the material!!!

Who Should Attend

- Hardware Practical Engineers, Design Engineers, Team Leaders and Project Managers

Course Contents

Signal Integrity

- Introduction – What is Signal Integrity
- Signal Integrity Noise Problems
- Contemporary technologies & Signal Integrity Problems
- What is High Speed?
- Signal Integrity Analysis in the Design Flow
- Signal Integrity Engineer in a Design Team

Transmission Lines

- What is Characteristic Impedance?
- Basic Transmission Line Theory
- Why use 50[Ohm] impedance?
- Termination Techniques
- Examples of solving "daily problems"

Crosstalk

- What is Crosstalk
- Identifying the mutual coupling causes
- Mutual Inductance and Capacitance
- PCB Trace Inductance and Capacitance
- Calculating the Crosstalk between signal traces
- The crosstalk coefficient
- Example – Using a Crosstalk Calculator
- Crosstalk in Differential Signals

Skin Effect

- What causes Skin Effect
- Skin depth
- Skin depth simulation results
- DC and AC resistance due to Skin Effect

Power Integrity

- What is Power Integrity?
- Review of capacitor types and their parameters

- Decoupling Capacitors & Parasitic elements
- Calculating the Decoupling Capacitor Value
- Decoupling & System Bandwidth
- VCC-GND plane capacitance
- Parasitic elements caused by PCB layout – Loop Inductance
- Via capacitance
- Via Inductance
- Introduction to Power Integrity Simulators & examples
- High Frequency Noise Isolation
 - Ferrite Bead Types
- Power Supply Filtering for Clock sources
- PI filter
- What is Ground Bounce?
- The affect of Ground Bounce on your circuit
- Techniques to decrease Ground Bounce
- Predicting Ground Bounce Magnitude

PCB Materials – The Signal Medium

- Dielectric Constant – What is Permittivity
- Dielectric Constant of various PCB materials
- PCB Materials and Resistive/Dielectric Losses
- Loss Tangent vs. Temperature and Moisture
- Conformal Coating
- Characteristic Impedance calculation for
 - Microstrip
 - Embedded Microstrip
 - Stripline
 - Asymmetric Stripline
 - Dual Stripline
 - Differential Stripline
 - Differential Microstrip
- Controlled Impedance Calculator - Demo
- Propagation Time for Microstrip and Stripline

EMC

- Introduction to EMC
- Return Paths – Low Speeds
- Return Paths – High Speeds
- How does the current return?
- Current Density in the Return Path
- The definition of Inductance and its relation to EMC
- Inductance and Antennas

- Inductance of signal path using Solid Reference Planes
- Inductance of signal path using Slotted Reference Planes
- Changing PCB Layers and its affect on the return path
- Connecting two or more PCBs through a connector and the return path
- VCC as reference plane
- Eddy Currents
- Slotted VCC planes and Gap Capacitors
- Edges of Planes
- Solder Pad Discontinuity
- Crosstalk and EMC
- The affect of decoupling on EMC
- Board Stack Up
- Reducing the Number of PCB Layer Trade Offs
- EMC, EMI and EMS – Definition of terms
- EMC Standards
- Checklist for EMC Compliance

Contemporary High Speed Technologies

- Introduction to High Speed Technologies
- Introduction to Differential Signals, advantages and disadvantages
- Technologies, LVDS, LVPECL, CML
- Interfacing between technologies
 - Active Interfacing
 - Passive Interfacing
 - Examples
- What is Jitter
 - Why Measure Jitter
 - Jitter vs. Wander
 - Definition of Jitter Parameters
 - Unit Interval (UI)
 - Characterizing Jitter sources, (description & causes and way to avoid them)
 - Bounded / Deterministic
 - Unbounded / Random Jitter
 - Calculating total Jitter to support expected BER performance
 - Jitter Measurement Techniques
 - The Eye Diagram and histogram (Time Domain)
 - The Bathtub Plot
 - Frequency Domain analysis of Jitter content
 - Methods for measuring a system's response to Jitter
 - Summary with DEMO:
 - DEMO with Agilent Test & Measurement equipment

- Signal Conditioning techniques
 - Pre-Emphasis
 - De-Emphasis
 - Equalization
- Embedded Waveform Viewing Technologies
 - DEMO with the Vitesse Components and Evaluation Boards

PCB Design

- Introducing the guidelines for layout
- PCB Design Flow
- Right Angle Bends – How do we do it?
- Delay Lines and Matched Delays
- Routing differential pairs, how...
- The 20H Rule vs. Shielding Vias
- Gap Capacitors – What are they and when to use them?
- Ground Traces, when and how?
- Vertical vs. Horizontal signal trace layout
- How tightly must we control Impedance
- Power Islands
- Stack Up Design
- The GND plane – to split or not to split

PCB Manufacturing

- PCB manufacturing costs
- Blind & Buried vias when, how, tradeoffs, costs
- Test Coupons for Controlled Impedance
- V-cuts and V-grooves
- Choosing the right PCB Material for the Application
- Tips for mass production manufacturing

High Speed Simulators

- High Speed Simulation – Work Flow
- Introduction to contemporary Simulation tools and Simulator types
- Modeling and Models
- Using the right simulation model for the application
- How to Analyze the simulation Results
- Power Integrity Simulators
- Signal Integrity Simulation – DEMO
- A hands-on work-shop using the Cadence or Mentor Simulation Tools

DDR2 & DDR3

- Introduction to DDR2 Technology

- Comparison of DDR types
- How do we start working with DDRs?
- DDR standards – Jedec
- Signal groups in DDRs
- What is ODT?
- What is OCT?
- DDR drive strength
- The Vref rails
- Single Ended and Differential signal levels
- DDR connectors
- Routing examples

DC/DC Power Supply Topologies

- Introduction to switched and non switched DC/DC topologies
 - Advantages and Disadvantages
- LDOs
- Buck Topology
- Synchronous Buck Topology

Summary